EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	390	(712/226).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/06 15:32
S2	3	(predicate$1 near4 (mov$3) near4 valu$3) and (register$1 near4 renam$3) and retir$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/06 15:32
S3	3	(predicate$1 near4 (mov$3) near4 valu$3) and (register$1 near4 renam$3) and retir$4	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/06 15:35
S4	35	(predicate$1 near4 instruction$1) and (register$1 near4 renam$3) and retir$4	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/06 15:57
S5	12	(predicate$1 near4 instruction$1) same ((register$1 near4 renam$3) and retir$4)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/11 08:09
S6	8	(predicate$1 near4 instruction$1) and (register$1 near4 renam$3) and retir$4 and (trac$3 near4 cach$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/06 15:58
S7	1	(guard$3 near4 instruction$1) same ((register$1 near4 renam$3) and retir$4)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/11 08:09
S8	12	(guard$3 near4 instruction$1) and ((register$1 near4 renam$3) and retir$4)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/11 08:11
S9	1	(register near4 renam$3) near4 (trace adj1 cach$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/11 08:12
S10	5	(register near4 renam$3) with (trace adj1 cach$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/11 08:14
S11	30	(register near4 renam$3) same (trace adj1 cach$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/11 08:14

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S12	0	predicat$3 near4 "if"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/11/09 16:16
S13	87	predicat$3 near4 conditional near4 branch$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/11/09 16:17
S14	58	predicat$3 near4 (conditional adj1 branch$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/11/09 16:17
S15	426	(712/226).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/21 09:40
S16	449	(712/226).CCLS.	US-PGPUB; USPAT	OR	OFF	2007/03/21 09:40
S17	92	predicat$3 near4 conditional near4 branch$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/21 09:41
S18	0	(predicat$3 near4 conditional near4 branch$3) same (register$1 near4 renam$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/21 09:41
S19	1	(predicat$3 with (conditional near4 branch$3)) same (register$1 near4 renam$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/21 09:43
S20	25	predicat$3 with (register$1 near4 renam$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/21 09:43
S21	28	(kottapalli-sailesh$).in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/24 22:15

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S Mahlke
W Chen
D Lin
R Hank
R Bringmann

Effective Compiler Support For Predicated Execution Using The Hyperblock - group of 10 »
SA Mahlke, DC Lin, WY Chen, RE Hank, RA Bringmann - Microarchitecture, 1992. MICRO 25., Proceedings of the 25th ..., 1992 - ieeexplore.ieee.org
... The condition for nullification, the **predicate**, is stored in a **predicate register** file and is specified via, an ad- ditional source operand added to each ...
Cited by 407 - Related Articles - Web Search - BL Direct

Facilitating superscalar processing via a combined static/dynamic **register renaming** scheme - group of 3 »
E Sprangle, Y Patt - Microarchitecture, 1994. MICRO-27. Proceedings of the 27th ... - ieeexplore.ieee.org
... We show that a statically defined tag ISA is better suited for a superscalar processor that supports **register renaming** for at least three reasons. ...
Cited by 30 - Related Articles - Web Search

Itanium processor microarchitecture - group of 45 »
H Sharangpani, H Arora - Micro, IEEE, 2000 - ieeexplore.ieee.org
... Scoreboard, **predicate** NaTs ... onto physical registers used to access the **register** file ... The dispersal and **renaming** hardware exploits high-level semantic information ...
Cited by 96 - Related Articles - Web Search - BL Direct

Enhanced Modulo Scheduling For Loops With Conditional Branches - group of 4 »
NJ Warter, GE Haab, JW Bockhaus, K Subramanian - Microarchitecture, 1992. MICRO 25., Proceedings of the 25th ..., 1992 - ieeexplore.ieee.org
... between predicates <p, F> and <p,T>. Also note that the **predicate** merge operation ... not shown in Figure 3 since they are removed by **register renaming** during mod ...
Cited by 76 - Related Articles - Web Search - BL Direct

Code Generation Schema For Modulo Scheduled Loops - group of 4 »
BR Rau, MS Schlansker, PP Tirumalai - Microarchitecture, 1992. MICRO 25., Proceedings of the 25th ..., 1992 - ieeexplore.ieee.org
... Hardware support for modulo scheduling includes rotating **register** files (**register** files which support compiler-managed **register renaming**, also known as the ...
Cited by 85 - Related Articles - Web Search - BL Direct

Dynamic hammock predication for non-predicated instruction set architectures - group of 17 »
A Klauser, T Austin, D Grunwald, B Calder - Proceedings of the 1998 International Conference on Parallel ..., 1998 - doi.ieeecomputersociety.org
... 2.3 Scheduler Support The **register** scheduling logic, for the ... Us- ing the **renaming** mechanism described in the ... If the **predicate** arrives before both of the use ...
Cited by 34 - Related Articles - Web Search

Introducing the IA-64 architecture - group of 48 »
J Huck, D Morris, J Ross, A Knies, H Mulder, R ... - Micro, IEEE, 2000 - ieeexplore.ieee.org
... AR BR FR GR PR Application **register** Branch **register** Floating-point **register** General **register Predicate register** ... Op **Register 1 Register 2 Register 3 Predicate** ...
Cited by 78 - Related Articles - Web Search - BL Direct

Predicate prediction for efficient out-of-order execution - group of 11 »
W Chuang, B Calder - Proceedings of the 17th annual international conference on ..., 2003 - portal.acm.org
... By performing **predicate** prediction before **register renaming** occurs, we predict which **predicate** paths will be true and which will be false. ...
Cited by 9 - Related Articles - Web Search

Optimizing Software Data Prefetches with Rotating Registers - group of 4 »
G Doshi, R Krishnaiyer, K Muthukumar - ieeexplore.ieee.org
... to the lowest numbered **register** after **renaming**, thus exhibiting ... architecture, a subset of the **register** files (General ... f32-f 127, and **predicate** registers p16-p63 ...
Cited by 26 - Related Articles - Web Search

Path Analysis and **Renaming** for Predicated Instruction Scheduling - group of 19 »
L Carter, B Simon, B Calder, L Carter, J Ferrante - International Journal of Parallel Programming, 2000 - Springer
... The **renaming** required by PSSA and PSpec also ... ISA (Playdoh) supports 4 **register** files: general purpose, floating point, branch, and **predicate**. ...
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